

CLAIMS

1. Field-effect microelectronic device,
including:

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a) a substrate,

b) at least one structure forming one or
more channels capable of connecting, in the direction
of their lengths, one or more sources and one or more
drains, which structure is formed by a stack, in a
10 direction orthogonal to a main plane of the substrate,
of at least two bars having different widths producing
a serrated profile.

2. Microelectronic device according to claim
15 1, said profile of the structure being a crenellated
profile.

3. Microelectronic device according to one
of claims 1 or 2, the stack including at least two
20 successive bars based on different materials.

4. Microelectronic device according to one
of claims 1 to 3, the stack including only bars capable
of providing electrical conduction.

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5. Microelectronic device according to one
of claims 1 to 3, the stack including one or more bars
capable of providing electrical conduction and one or
more non-conductive bars.

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6. Microelectronic device according to claim 5, the stack including an alternation of bars capable of providing electrical conduction and non-conductive bars.

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7. Microelectronic device according to one of claims 1 to 3, the stack including at least two successive bars based on different semiconductive materials and/or having different dopings.

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8. Microelectronic device according to one of claims 1 to 3, the stack including at least two successive bars of which one is based on a semiconductive material and the other is based on an insulating material.

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9. Microelectronic device according to claim 7, the stack including at least two successive bars of which one is based on Si and the other is based on SiGe.

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10. Microelectronic device according to one of claims 5 or 6, the stack including at least two successive bars of which one is based on Si and the other is based on SiO₂.

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11. Microelectronic device according to one of claims 1 to 10, at least one of the bars being at least partially surrounded, in a direction parallel to a main plane of the substrate, with insulating caps.

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12. Microelectronic device according to claim 11, said insulating caps being based on nitride.

13. Microelectronic device according to one
5 of claims 1 to 12, said structure including at least two bars having different lengths and/or different thicknesses.

14. Microelectronic device according to one
10 of claims 1 to 13, also including a hard mask on said stack.

15. Field-effect microelectronic device according to one of claims 1 to 14, also including : a
15 gate at least partially covering said structure and optionally the hard mask.

16. Field-effect microelectronic device according to one of claims 1 to 15, also including :
20 one or more sources connected by said structure to one or more drains.

17. Field-effect microelectronic device,
including:
25 a) a substrate,
b) at least one structure forming one or more channels capable of connecting, in the direction of their lengths, a single source and a single drain, which structure is formed by a stack, in a direction
30 orthogonal to a main plane of the substrate, of at

least two bars, based on different materials and/or having different widths.

18. Method for producing a field-effect
5 microelectronic device equipped with at least one structure comprising at least two stacked bars, of different widths, capable of forming one or more transistor channels, characterised in that said method includes the steps of:

- 10 - forming, on a substrate, a stack of a plurality of layers comprising at least two successive layers based on different materials,
- forming at least one mask on said stack,
- anisotropic etching of the layers through
15 the mask,
- partial and selective etching of one or more layers of the stack.

19. Method according to claim 18, said stack
20 including at least two layers based on different semiconductive materials or having different dopings.

20. Method according to one of claims 18 or 19, said stack including at least one Si-based layer
25 and at least one SiGe-based layer.

21. Method according to one of claims 18 to 20, said stack including at least one layer based on an insulating material and one layer based on a
30 semiconductive material.

22. Method according to one of claims 18 to 21, also including : the conformal deposition of a dielectric layer on said structure.

5 23. Method according to claim 22, said dielectric layer being based on nitride.

24. Method according to one of claims 22 or 23, also including : the partial isotropic etching of
10 said dielectric layer, so as to form insulating caps around certain bars of said structure.

25. Method according to one of claims 18 to 24, also including : the formation of a gate at least
15 partially covering said structure and optionally the hard mask.

26. Method according to claim 25, the formation of the gate including steps consisting of:

- 20 - covering the structure with an insulating layer,
- forming at least one opening in the insulating layer so as to expose said structure,
- covering the structure with a gate
25 insulating layer,
- filling the opening with a gate material.

27. Method according to one of claims 25 or 26, including, prior to the formation of the gate: one
30 or more steps in which said structure is doped.